LOW LEAKAGE CMOS POWER MUX

ABSTRACT

A power supply multiplexing circuit including a first supply voltage input. A first pair of cascoded PMOS transistors are in series with the first supply voltage input. A first native NMOS transistor is in series with the first pair of cascoded PMOS transistors. Also, a second supply voltage input and a second pair of cascoded PMOS transistors are in series with the second supply voltage input; and a second native NMOS transistor in series with the second pair of cascoded PMOS transistors. The gates of the first and second native NMOS transistors are driven by two control signals out of phase with each other, and sources of the first and second native NMOS transistors are connected together to output an output voltage.

165604_1.DOC